AMENDMENTS TO THE SPECIFICATION

[REPLACEMENT 0018] The receiver module is provided with a low-cost digital CMOS integrated circuit chip for processing the I and Q sigma delta bit streams and baseline crossing countable pulse streams produced by the CMOS receiver chip. The digital circuit includes logic, memory, digital filter and digital arithmetic circuits for downsampling ~~the downsampling~~ the sigma delta I and Q bit streams to produce signed 8-bit I and Q data sampled at a rate nominally equivalent to 2X the power line frequency. The sampling rate clock is obtained by integer division of the 32,760 Hz system clock where the division ratio is "dithered" to establish and maintain receiver module phase locking with the phase of the transmitter modulation signals. The digital chip also provides digital correlation of 8 successive I and Q sampled data sets to extract sets of sample measures of the separately identifiable portions of the I and Q received baseband signals resulting from the separately identifiable magnetic field intensity components broadcast by the transmitter first, second and third antennas. The 8-set correlations are clocked by a measurement rate clock which is the sampling clock divided by eight and therefore nominally ¼ the power line frequency. The correlations are done with a simple and compact digital addition or subtracting means whereby each I or Q data sample needs to be accumulated only once per measurement cycle. Although the correlations are done with simple digital means, the results match very closely with ideal continuous time correlation since the sigma delta modulators employ continuous time integrators and the reference waveforms for matched filter correlation are all symmetric, unit amplitude square waves such that correlation by adding or subtracting is exactly equivalent to continuous time correlation. In addition to providing nearly ideal matched filter extraction of the separately identifiable magnetic field component measures, the correlation filters also provide near ideal rejection of power line interference components because the reference correlation waveforms are coherent and integral sub-harmonics of the power line frequency. Additionally, the correlation filtering process provides complete rejection of any dc components in the I and Q signal samples.

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[REPLACEMENT 0019] The digital chip also provides for post processing of the I and Q correlation results to obtain first, second and third power measures corresponding to those portions of the received signal power arising respectively from the separately identifiable magnetic field power components broadcast by the transmitter first, second and third antennas. These relative values of the computed power measures ~~is~~ are dependent on the orientation of the sensing antenna relative to the direction vector of the incident magnetic field. Computing means is also provided for digitally summing the first, second and third power measures to obtain a digital measure of the total incident magnetic field power ~~which is substantially independent of the orientation of the sensing antenna~~ and therefore useful for accurate and robust wireless boundary proximity detection. The digital chip also provides post processing of certain correlation results to compute quadrature pseudo power variables that are measures of only that portion of the received signal power arising from magnetic field power components broadcast by the transmitter first antenna. Because of the cross-correlation properties previously discussed, these quadrature pseudo power measures exhibit very low sensitivity to power line frequency interference and also very low sensitivity to I and Q signal components corresponding the signals broadcast from the transmitter second and third antennas. These pseudo power measures, therefore, provide a very robust data-based means for dithering the sampling rate clock to achieve and maintain a prescribed phase lock between the phase of the digital chip measurement clock and the phasing of the magnetic field modulation signals. Because the correlation phase locking is based on the transmitter first modulation signal, it is important that the two-axis sensor antenna be arranged to have some non-zero response to the component of the magnetic field that is broadcast by the transmitter first antenna, at least during those times that the receiver module needs to be accurately monitoring proximity to the wireless boundary. This is arranged in pet containment applications, for example, by orienting the transmitter 3-axis broadcasting antenna such that the principal axis of the transmitter first antenna is in the horizontal plane and by mounting the receiver module sensing antenna on the pet such that its principal sensing plane is

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nominally horizontal when the pet is in an upright position from which it might walk or run toward the wireless boundary.

[REPLACEMENT 0052] Figure 3a illustrates one embodiment of the transmitter **10** including a carrier signal generator **15** for the production of three separately identifiable carrier signals **50**, **51**, and **52,** which are modulated using binary phase-shift keying (BPSK). Antenna drivers **47**, **48** and **49**, which continuously and simultaneously excite a 3-axis antenna arrangement **13**, amplify the carrier signals **50, 51 and 52**. The antenna arrangement **13** continuously broadcasts the time varying, composite magnetic field **12**. The antenna arrangement **13** generally includes a geometrically orthogonal set of three separate antenna elements consisting of a first antenna **43** having a principal axis **40** and excited by the amplified version of a first BPSK modulated carrier signal **50**, a second antenna **44** having a principal axis **41** and excited by the amplified version of a second BPSK modulated carrier signal **51** and a third antenna **45** having a principal axis **42** and excited by the amplified version of a third BPSK modulated carrier signal **52**. The desired signal voltage amplitudes produced by the antenna drivers **47**, **48** and **49** are boosted by exciting the antenna elements **43**, **44** and **45** in a conventional series resonant mode made possible by the use of resonating capacitors **68**, **69** and **70**. The three, separately identifiable BPSK modulated carrier signals **50**, **51** and **52** are generated on the signal generator **15** by the BPSK modulator circuits **53**, **54** and **55**, which modulate a common carrier signal **56** with separately identifiable square wave modulation signals **57**, **58**, and **59**. The modulation signals **57**, **58** and **59** are digitally synthesized from a master clock signal **64** by the respective digital signal generation circuits **60**, **61** and **62**. The frequency synthesis circuit **17** which uses conventional phase locked loop methods for frequency control and includes an analog circuit for making the amplitude of the carrier frequency signal **56** vary in proportion to a reference voltage applied to an amplitude control input **65**, synthesizes the carrier frequency signal **56** from the master clock signal **64**. The carrier frequency **56** produced by the synthesis circuit **17** is tuned to a selected one of numerous possible carrier frequencies using an appropriate *n*-bit digital code applied to the digital frequency control input lines **73**. The *n*-bit digital

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code controlling the carrier frequency selection is pin-programmed after the signal generator **15** is fabricated. In the illustrated embodiment, the control lines **73** of the signal generator **15** are connected to an off-chip array **71** of *n* connections **72** each of which can be set to a logical "one" or "zero" as desired. Because the carrier signals **50**, **51** and **52** are all produced from the same carrier signal **56**, the magnetic field power components simultaneously broadcast from each of the antenna elements **43**, **44** and **45** are corporately and proportionately increased or decreased by connecting the amplitude control line **65** to an off-chip means for manually adjusting the voltage bias on the amplitude control line **65**. Manual adjustability of the voltage applied to amplitude control input **65** is optionally provided for by connecting the control line **65** to an off-chip voltage divider circuit **66** consisting of a potentiometer connected to the power supply voltage **67** or to some other suitable bias voltage. The expanse **20** of the wireless boundary, defined by the locus of all points on a path surrounding the transmitter **10** for which the total power in the composite magnetic field is a constant, is thus increased by adjusting the voltage divider **66** to effect an increase in the amplitude of the carrier signal **56** and the expanse **20** is similarly decreased by adjusting the voltage divider **66** to effect a decrease in the amplitude of the carrier signal **56**.

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[REPLACEMENT 0075] The measures XS **384** and ZS **386** represent accurate power measures only if the receiver module f_M measurement clock **316** is locked in close phase alignment with the transmitter third modulation signal **59**. However, the power measure YS **382** is accurate irrespective of the phase relationship between the receiver module acquisition and measurement clock, f_M **316** and transmitter modulation signals. The digital arithmetic logic unit **304** also processes the indicated correlation results **320** according to the arithmetic formula **376** of Figure 10c to produce a first pseudo power measure, Y1S **324a** and for processing the indicated correlation results **320** according to the arithmetic formula **378** of Figure 10c to produce a second pseudo power measure, Y2S **324b**. The pseudo power measures **324a** and **324b** have variable magnitude as a function of the phase of the receiver module f_M clock relative to the phase of the transmitter first modulation signal **57**, however the variation of measure **324a** is in

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quadrature relationship with the variation of measure **324b**. Moreover, the magnitudes are equal when the phase of the f_M clock **316** is aligned with the phase of the transmitter third modulation signal **59** as desired to guarantee the accuracy of power measures **384** and **386** as previously described. Moreover any shift away from this desired phase lock relationship produces an increase in the magnitude of the **324a** pseudo power measure and a decrease in the magnitude of the **324b** pseudo power measure or vice versa. The magnitude difference between the pseudo power measures **324a** and **324b** is therefore useful for application as an error signal in a dithering feedback means of maintaining the desired phase lock between receiver module f_M clock **316** and transmitter third modulation signal **59**. The frequency of the f_S sampling clock **314** is dithered by dithering the N_{DIV} ratio used by the I/Q sample rate generator **34** to produce the f_S clock. As previously discussed, the f_S clock is desired to be nominally 2X the power line frequency so that the f_M clock is ¼ the power line frequency to be in agreement with the frequency of the transmitter first modulation signal **57**. If Y2S < Y1S as detected by the data phase locking logic **306**, then N_{DIV} is set to provide an f_S slightly less than twice the power line frequency. If the data phase locking logic **306** determines that Y2S > or = Y1S, then N_{DIV} is set to provide an f_S slightly greater than twice the power line frequency. If the noisy data detection logic **310** determines that the Y1S and Y2S measures **324** are based on noisy and potentially invalid data, then N_{DIV} is not dithered, but is held at the nominal settings. The dithering data phase lock process uses the N_{DIV} values as revealed in the truth table **400** of Figure 10d and is effective to acquire the desired data phase locking in about 1 second and to maintain robust locking properties under poor signal-to-noise ratio conditions. To ensure that all 8 sets of I/Q data samples **355** used in a given correlation operation are acquired with the same sampling time **315**, the value of N_{DIV} must be dithered sometime **354** or **362** before the completion of the sample period corresponding to the acquisition of the first data set I0/Q0 **352** or **358**. This means that the arithmetic logic unit **304** must complete the calculation of the pseudo power measures **324** in less than 8.33 milliseconds (for the case of 60 Hz line power frequency) which corresponds to about 273 cycles of the 32,760 Hz system clock **28**. This is achieved using a Booth multiplication procedure that

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requires only 10 clock cycles for multiplication of 8-bit numbers. Those skilled in the art will recognize other multiplication methods which can be used.